

Application Serial No. 10/787,499
Reply to Office Action of April 18, 2005

PATENT
Docket: CU-3609

Amendments To The Claims

The listing of claims presented below will replace all prior versions, and listings, of claims in the application.

Listing of claims:

1. (currently amended) A multi-chip package comprising:

a circuit substrate consisting of first, second, and third areas ~~which~~ wherein the circuit substrate is bent so that the first, second, and third areas surround three sides of the multi-chip package; and

at least two semiconductor chips which are positioned within an internal space of the package defined by the internal surfaces of the above three areas,

wherein the semiconductor chips are physically bonded and electrically connected to each other.
2. (original) The multi-chip package according to claim 1, wherein the circuit substrate comprises a plurality of substrate pads which are formed on the internal surfaces of the above three areas and electrically connected to the semiconductor chips.
3. (original) The multi-chip package according to claim 1, wherein the semiconductor chips comprises a plurality of chip pads formed on the top surfaces of the semiconductor chips and a plurality of chip bumps individually formed on each of the chip pads, respectively corresponding chip bumps and substrate pads being physically

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bonded and electrically connected to each other.

4. (original) The multi-chip package according to claim 1 or 3, wherein the semiconductor chips comprises a first semiconductor chip provided on the first area, at least one second semiconductor chip provided on the second area, and a third semiconductor chip provided on the third area.
5. (original) The multi-chip package according to claim 4, wherein a rear surface of the first semiconductor chip is faced to a rear surface of the third semiconductor chip.
6. (original) The multi-chip package according to claim 1, wherein the first semiconductor chip and the third semiconductor chip have an identical size.
7. (original) The multi-chip package according to claim 2, wherein the circuit substrate comprises a plurality of ball lands which are formed on the external surface of the first area and electrically connected to the substrate pads.
8. (original) The multi-chip package according to claim 7, further comprising a plurality of solder balls that are respectively formed on the ball lands.
9. (original) The multi-chip package according to claim 2, wherein the circuit substrate further comprises a fourth area that extends from a side of the third area.

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10. (original) The multi-chip package according to claim 9, wherein the fourth area comprises a plurality of contact pads which are formed on a side of the fourth area and electrically connected to the substrate pads.
11. (original) The multi-chip package according to claim 1, wherein the circuit substrate comprises a plurality of notches being formed in the external surfaces of first, second and third areas at the boundaries of these three areas.
12. (original) The multi-chip package according to claim 1 or 11, further comprising an encapsulant filled in the internal space of the package.